

# MT9435A

## P-Channel Enhancement Mode Field Effect Transistor

### Product summary

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (m $\Omega$ ) Typ
-30V	-5.6A	45@ V <sub>GS</sub> =-10V
		75 @ V <sub>GS</sub> =-4.5V

### Features

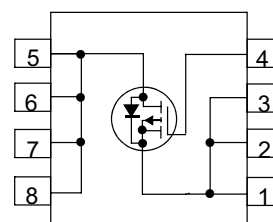
- Supper high dense cell design for low R<sub>DS(ON)</sub>
- Rugged and reliable
- Sample drive requirment
- SOP-8 package



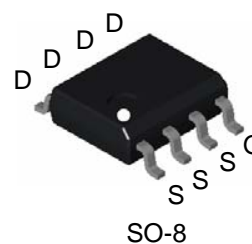
**MT Semiconductor®**

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### Simplified Schematic



### MARKING DIAGRAM & PIN ASSIGNMENT



### Absolute Maximum Ratings (T<sub>A</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	-30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous <sup>a</sup> @T <sub>j</sub> =125°C	I <sub>D</sub>	-5.6	A
- Pulse $d^b$	I <sub>DM</sub>	-24	A
Drain-source Diode Forward Current <sup>a</sup>	I <sub>S</sub>	-1.7	A
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	2.5	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> ,T <sub>STG</sub>	-55 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to Ambient <sup>a</sup>	R <sub>th JA</sub>	50	°C/W
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ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

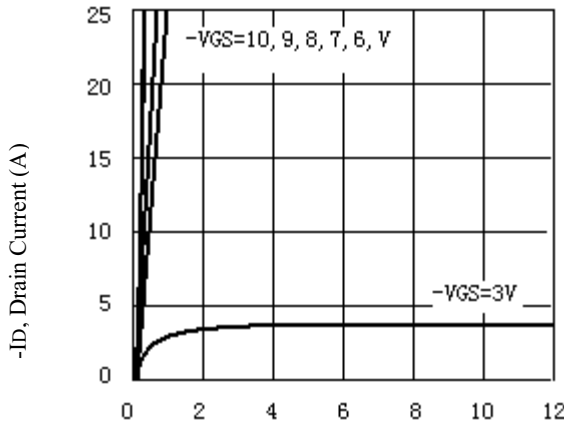
Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V,I <sub>D</sub> =-250μA	-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V,V <sub>GS</sub> =0V			-1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V			±100	nA
ON CHARACTERITICS						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =-250μA	-1	-1.5	-2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V,I <sub>D</sub> =-5.6A		45	55	m Ω
		V <sub>GS</sub> =-4.5V,I <sub>D</sub> =-4.2A		75	85	
Forward Transconductance	g <sub>FS</sub>	V <sub>GS</sub> =-5V,I <sub>D</sub> =-5.6A		5		S
DAYNAMIC CHARACTERISTICS						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-15V,V <sub>GS</sub> =0V f=1.0MHz		582		pF
Output Capacitance	C <sub>OSS</sub>			125		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			86		pF
SWITCHING CHARACTERISISTICS						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =-15V I <sub>D</sub> =-5.6A, V <sub>GEN</sub> =-4.5V R <sub>L</sub> =10ohm R <sub>GEN</sub> =10ohm		9		ns
Rise Time	t <sub>r</sub>			10		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			38		ns
Fall Time	t <sub>f</sub>			23		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-15V,I <sub>D</sub> =-1A V <sub>GS</sub> =-10V		11.7		nC
Gate-Source Charge	Q <sub>gs</sub>			2.1		nC
Gate-Drain Charge	Q <sub>gd</sub>			2.9		nC

ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

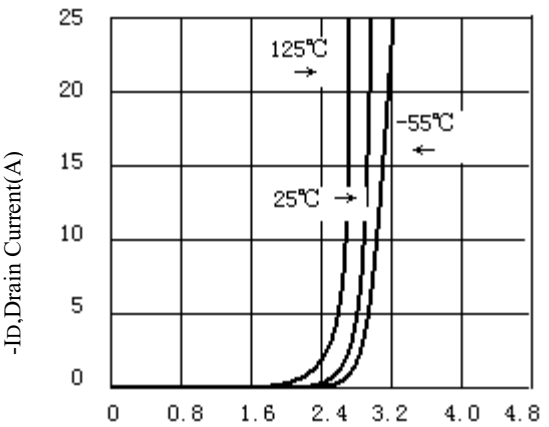
Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage	VSD	VGS=0V, IS=-1.7A		-0.84	-1.2	V

Notes

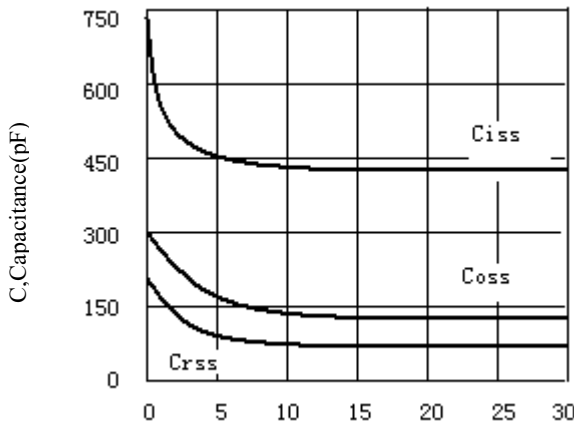
- Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$
- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
- Guaranteed by design, not subject to production testing.



- VDS, Drain-to-Source Voltage (V)  
Figure 1. Output Characteristics



-VGS, Gate-to-source Voltage (V)  
Figure 2. Transfer Characteristics



- VGS, Drain-to Source Voltage  
Figure3. Capacitance

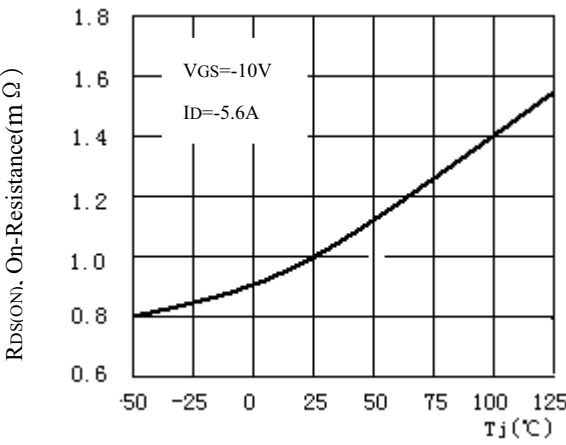


Figure4. On-Resistance Variation with Temperature

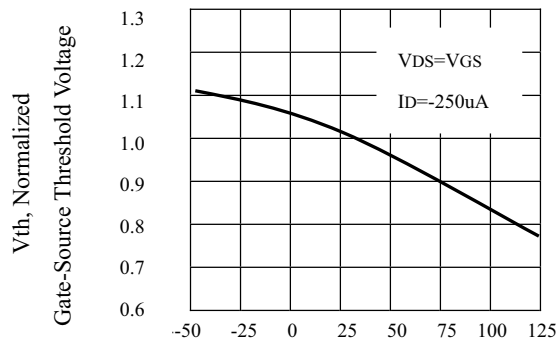


Figure 5. Gate Threshold Variation  
With Temperature

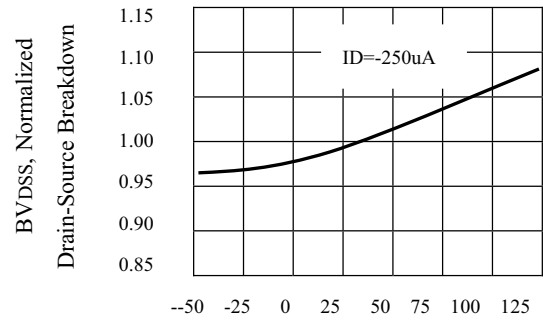


Figure 6. Breakdown Voltage Variation  
With Temperature

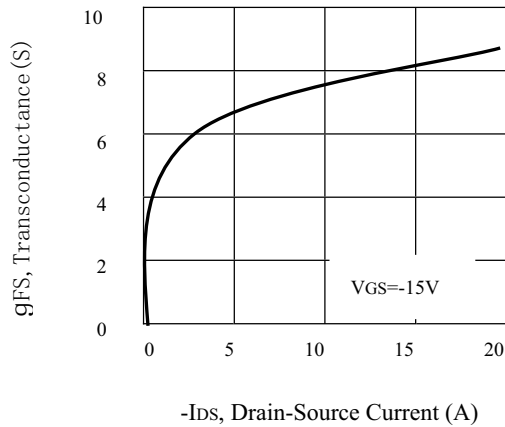


Figure 7. Transconductance Variation  
With Drain Current

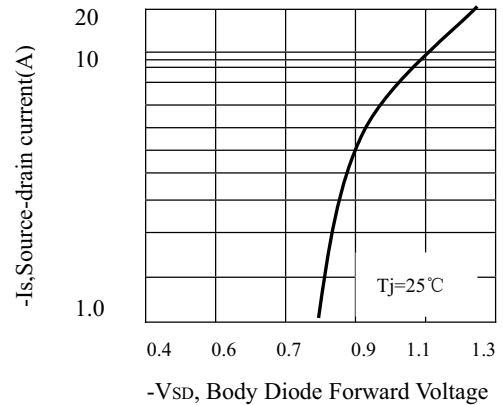


Figure 8. Body Diode Forward Voltage  
Variation with Source Current

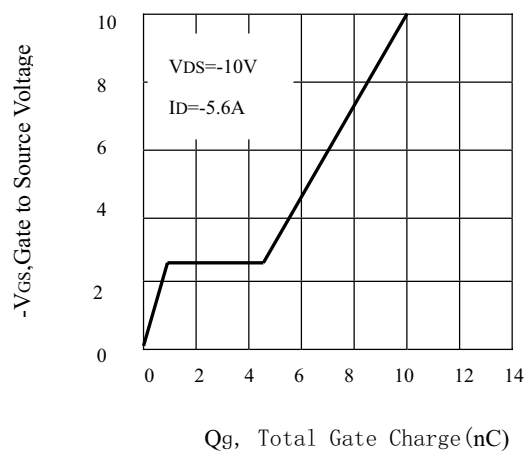


Figure 9. Gate Charge

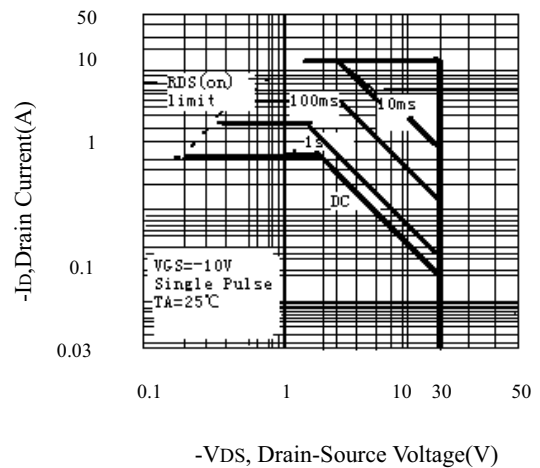


Figure 10. Maximum Safe Operating Area

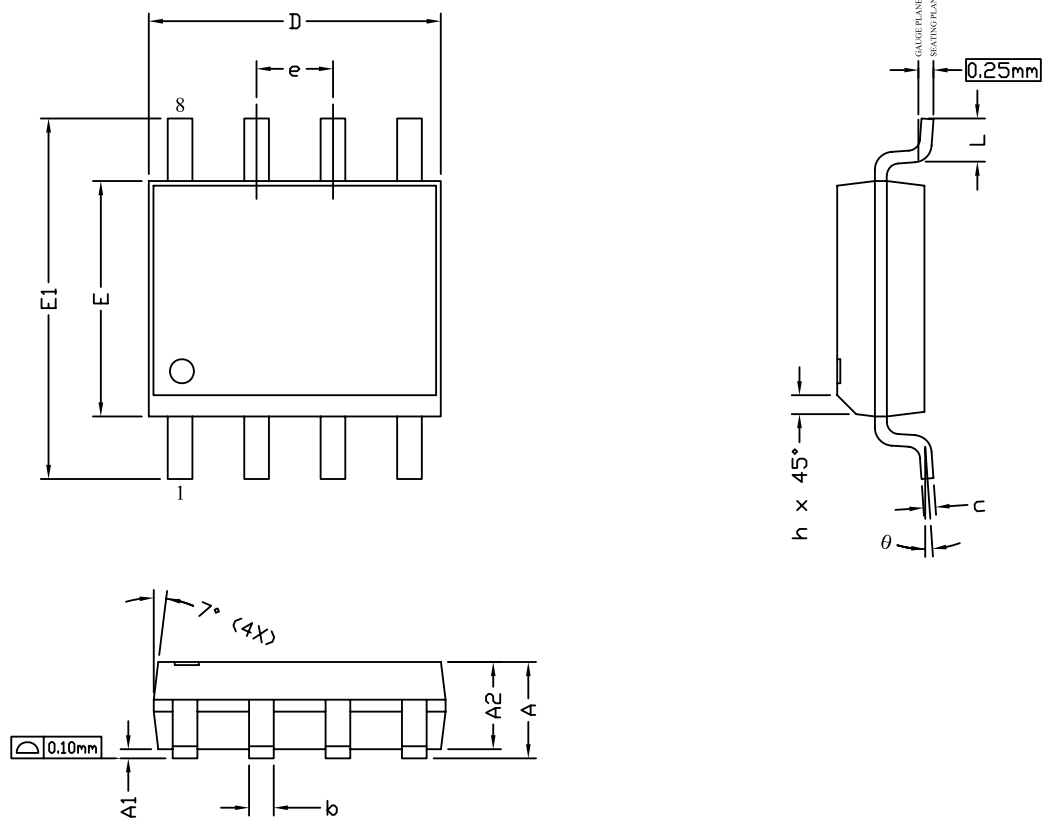
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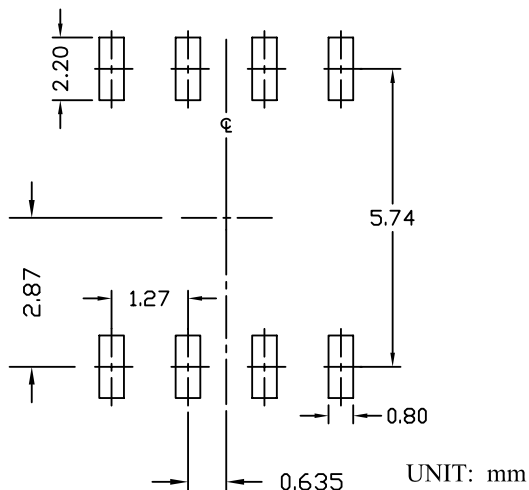
Version

rev H

## S08 PACKAGE OUTLINE



## RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
$\theta$	$0^\circ$	—	$8^\circ$	$0^\circ$	—	$8^\circ$

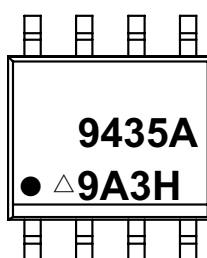
## NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.  
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

## Part Marking Information

### SO-8 (PMG Code )

SO-8 Devices



9435A = Example Base Part Number

● = Pin 1 Indicator

△ = ESD Symbol (⚡)

9 = Year Code

A = Month Code

3 = Week Code

H = Assembly Factory Code

**NOTE:**

1. For analog switches base part includes DG prefix. Package suffix may or may not be present, depending on room available.

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.

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