

MT8810E

Dual N-Channel Power MOSFET

General Description

This N-channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Features

- 20V, 7.5A $R_{DS(on)} = 18\text{ m}\Omega @ V_{GS} = 4.5\text{V}$
 $R_{DS(on)} = 22\text{ m}\Omega @ V_{GS} = 2.5\text{V}$
- Extended V_{GS} range ($\pm 12\text{ V}$) for battery applications
- High performance trench technology for extremely low $R_{DS(on)}$
- Low profile TSSOP-8 package

Applications

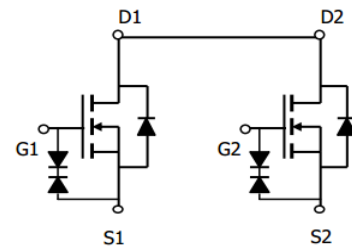
- Load switching
- Battery charge
- ESD Protection



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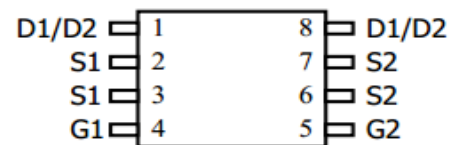
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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT

Top View



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	7.5	A
Drain Current-Pulsed (Note 1)	I_{DM}	30	A
Maximum Power Dissipation	P_D	1.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	83.3	$^\circ\text{C/W}$
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Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MT8810E	MT8810E	TSSOP-8	13"	12mm	2500 units

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =16V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.4	0.6	1.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =6A	-	18	21	mΩ
		V _{GS} =2.5V, I _D =5A	-	22	24	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =7A	-	20	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =10V, V _{GS} =0V, F=1.0MHz	-	1100	-	PF
Output Capacitance	C _{OSS}		-	185	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	165	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V, R _L =1.35Ω V _{GS} =5V, R _{GEN} =3Ω	-	5.5		nS
Turn-on Rise Time	t _r		-	14		nS
Turn-Off Delay Time	t _{d(off)}		-	48		nS
Turn-Off Fall Time	t _f		-	15		nS
Total Gate Charge	Q _g	V _{DS} =10V, I _D =7A, V _{GS} =4.5V	-	15		nC
Gate-Source Charge	Q _{gs}		-	0.7	-	nC
Gate-Drain Charge	Q _{gd}		-	3.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =1A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	7.5	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

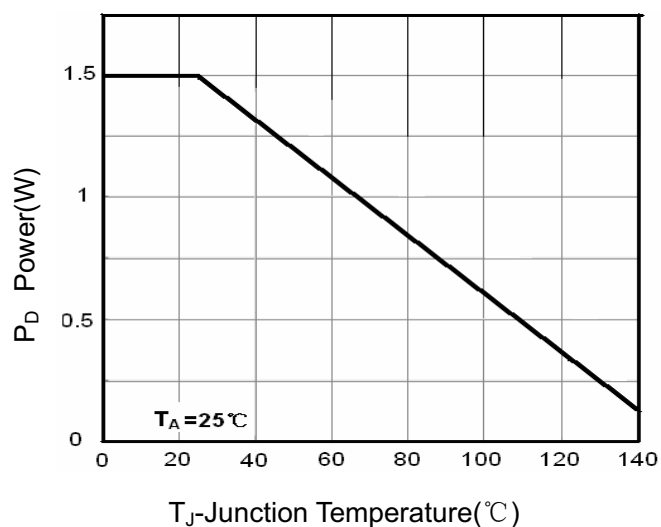


Figure 1 Power Dissipation

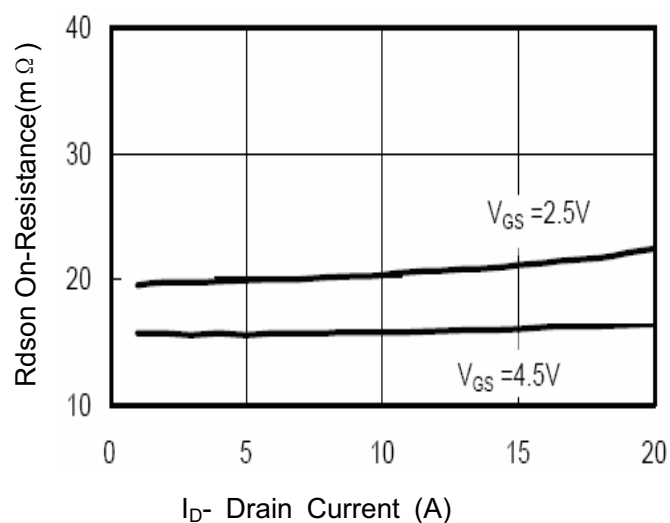


Figure 2 Drain-Source On-Resistance

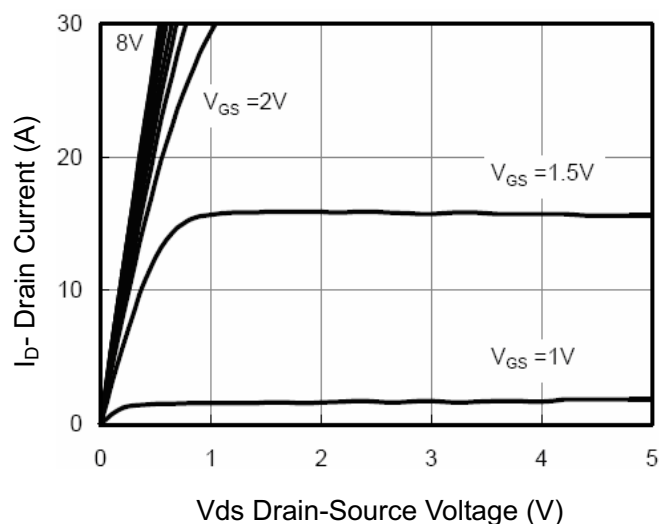


Figure 3 Output Characteristics

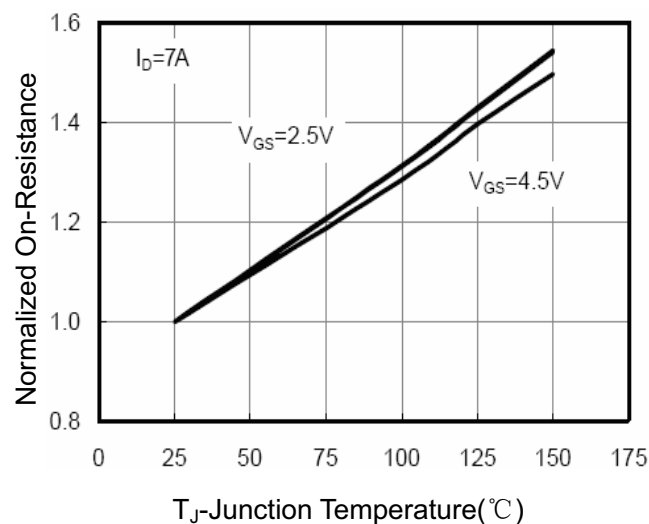


Figure 4 Drain-Source On-Resistance

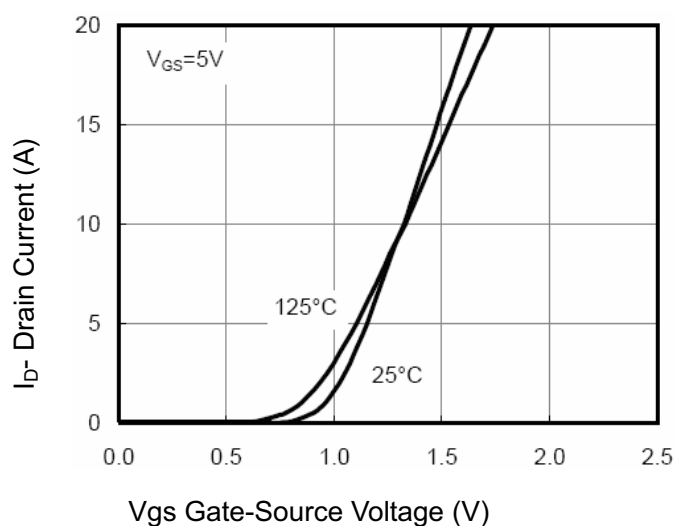


Figure 5 Transfer Characteristics

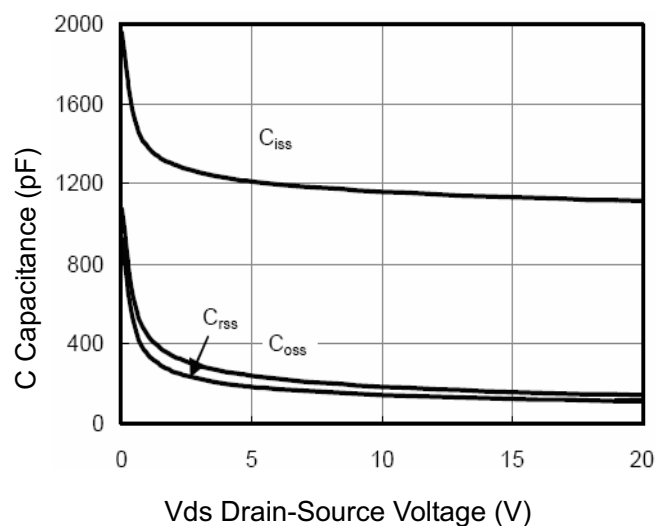


Figure 6 Capacitance vs V_{DS}

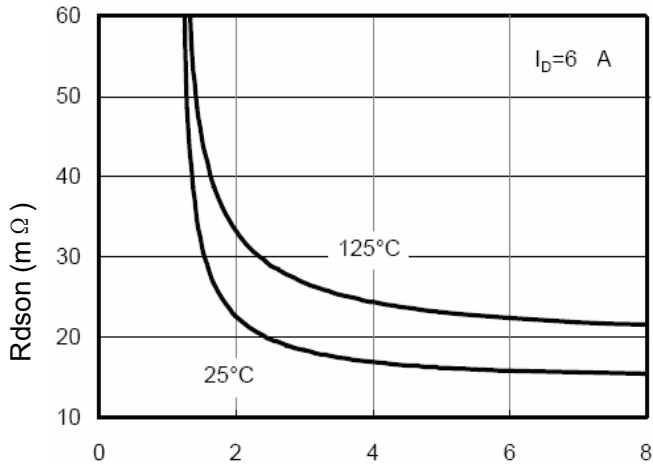


Figure 7 Rdson vs Vgs

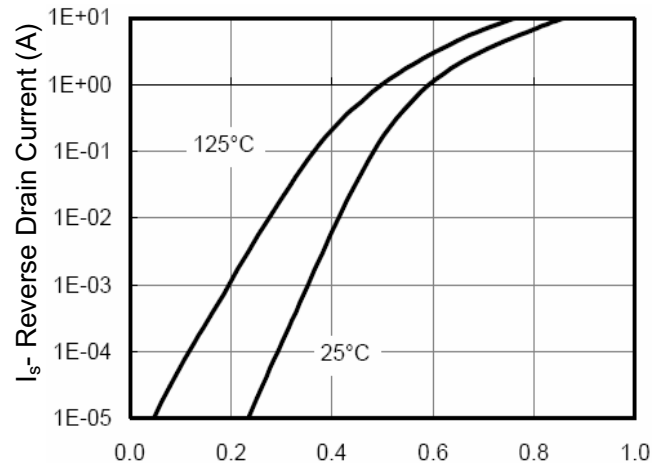


Figure 8 Capacitance vs Vds

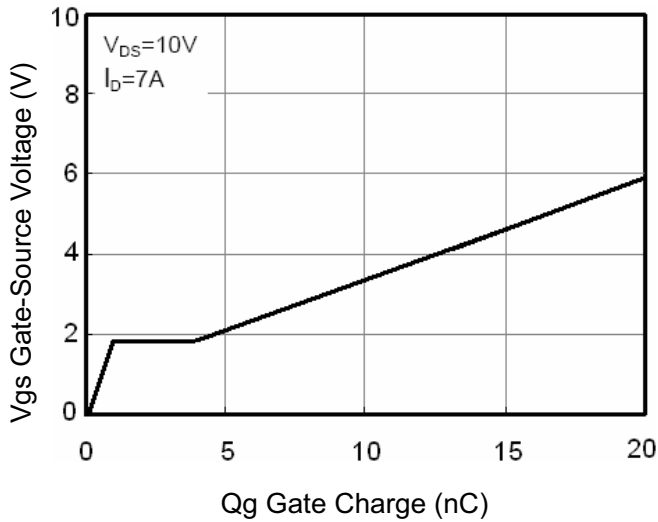


Figure 9 Gate Charge

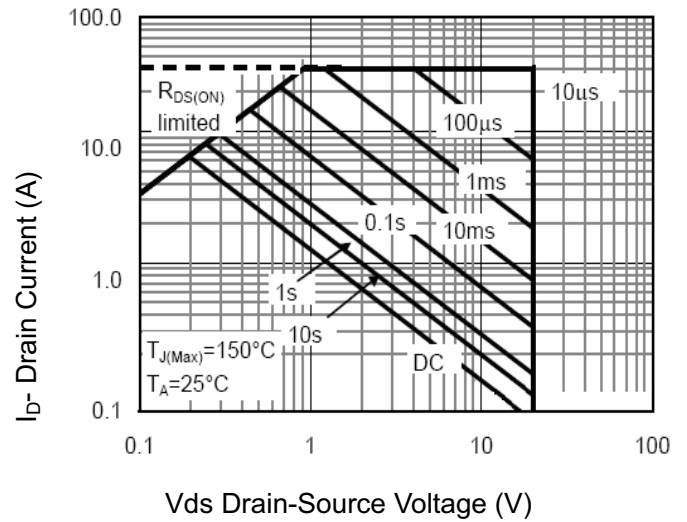


Figure 10 Safe Operation Area

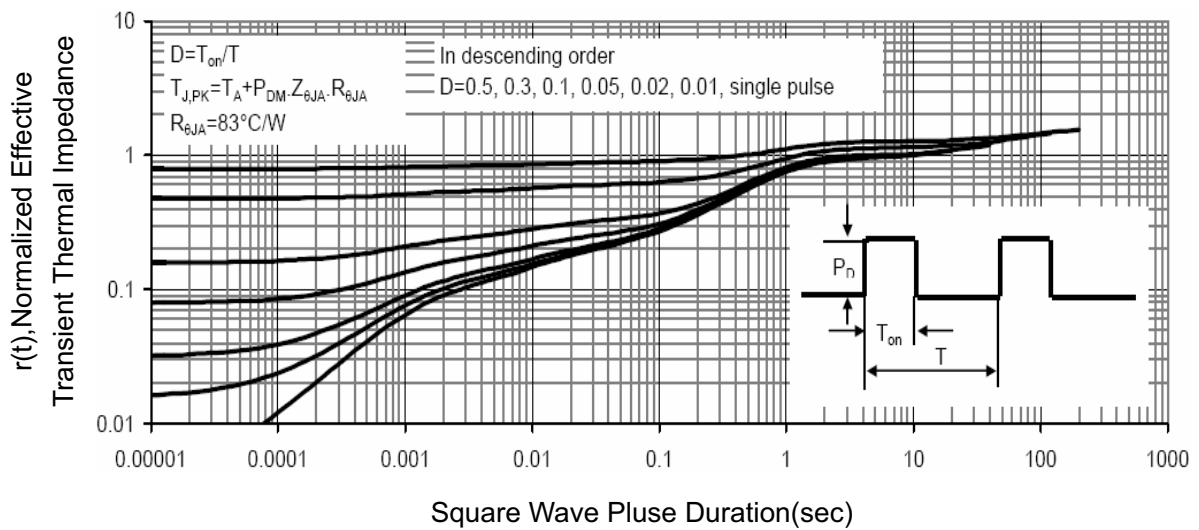


Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuits and Waveforms

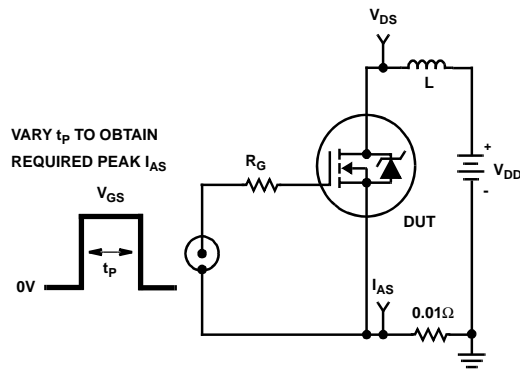


Figure 14. Unclamped Energy Test Circuit

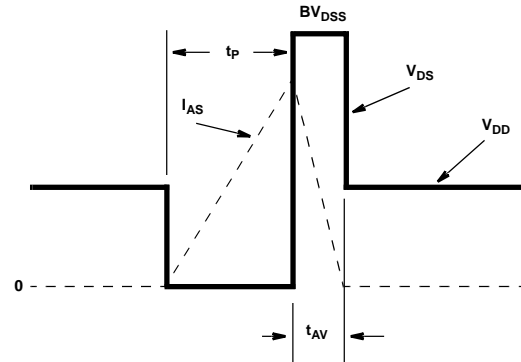


Figure 15. Unclamped Energy Waveforms

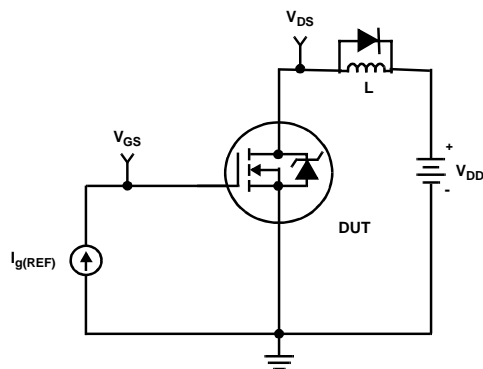


Figure 16. Gate Charge Test Circuit

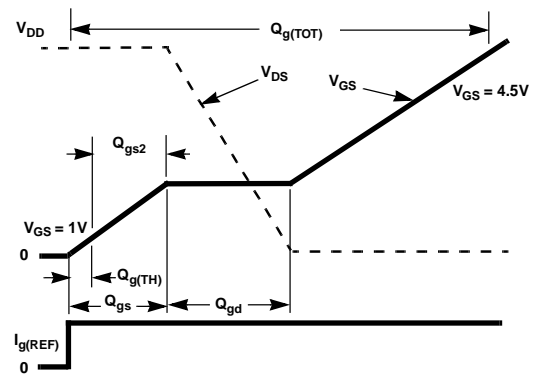


Figure 17. Gate Charge Waveforms

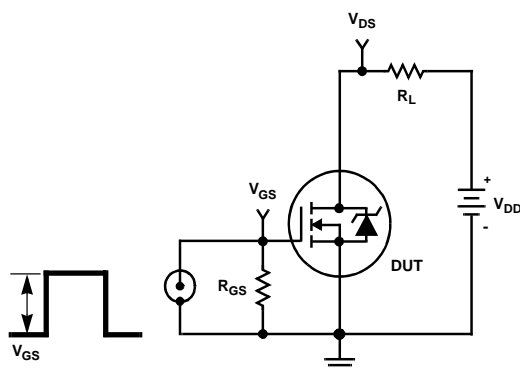


Figure 18. Switching Time Test Circuit

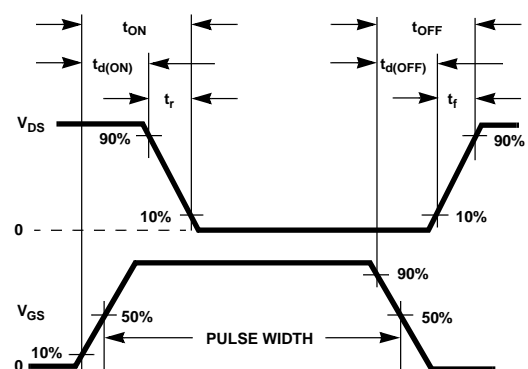
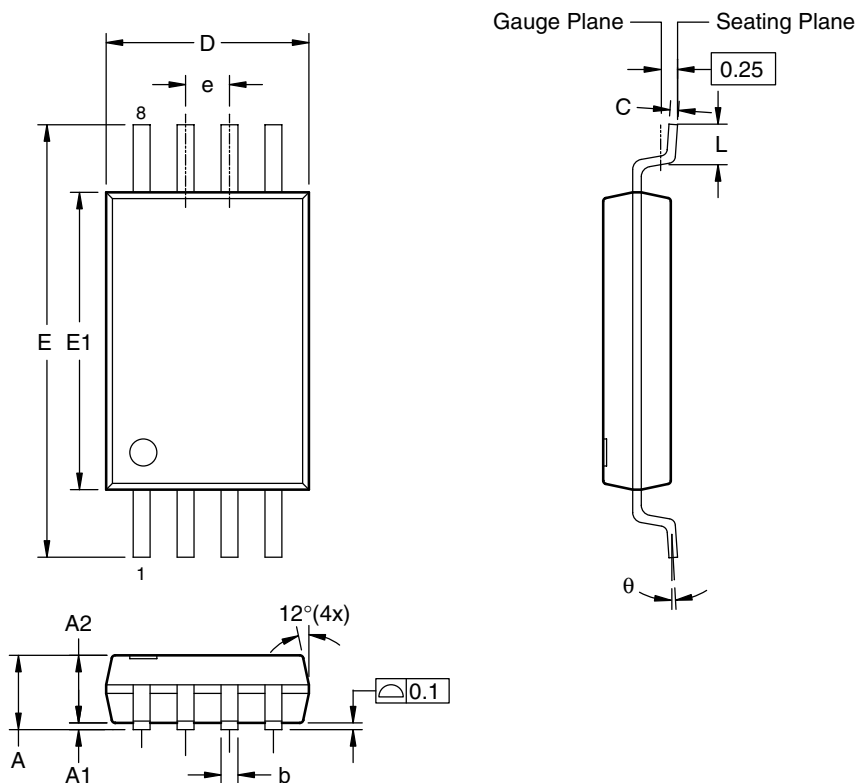
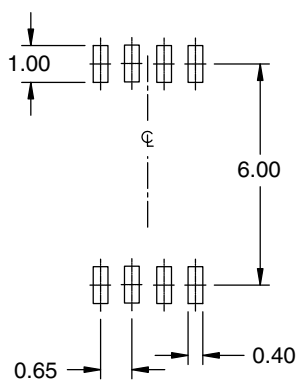


Figure 19. Switching Time Waveforms

TSSOP-8 Package Dimensions



RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	—	0.20
D	2.90	3.00	3.10
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	—	—	0.047
A1	0.002	—	0.006
A2	0.031	0.039	0.041
b	0.007	—	0.012
C	0.004	—	0.008
D	0.114	0.118	0.122
E	0.252 BSC		
E1	0.169	0.173	0.177
e	0.026 BSC		
L	0.018	0.024	0.030
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
6. Refer to JEDEC MO-153(AA).

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