# MT4638R

## General-Purpose Switching Device Applications

MT Semiconductor®

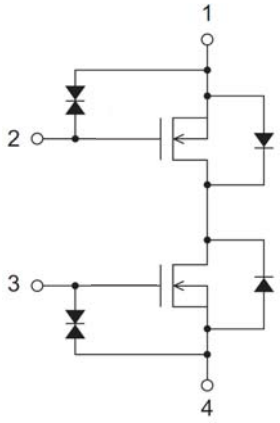
http://www.mtsemi.com

### Features

- Super high dense cell design for low RDS(ON)
- Rugged and reliable
- ESD Protected

| PRODUCT SUMMARY | | |
|---|---|---|
| VSSS | IS | RSS(ON) (mΩ) Max |
| 20V | 6A | 38.0 @ VGS=4.5V |
| | | 48.0 @ VGS=2.5V |
| | | 64.0 @ VGS=1.8V |

### Simplified Schematic




MARKING DIAGRAM & PIN ASSIGNMENT

### General Description

This N-Channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.It is ESD Protected.

### Applications

- Lithium battery protection board
- Bank of power

### MOSFET Maximum Ratings $T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{SSS}$ | Source to Source Voltage | | | 20 | V |
| $V_{GSS}$ | Gate to Source Voltage | | | ±12 | V |
| $I_D$ | Drain Curren | - Continuous (Silicon Limited) | $T_C$ = 25°C | 6 | A |
| | | - Continuous( Package Limited) | $T_C$ = 25°C | 10 | |
| | | - Continuous | $T_C$ = 25°C(Note 1a) | 30 | |
| | | - Pulsed | | 60 | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy | | (Note 3) | 1.0 | mJ |
| $P_D$ | Power Dissipation | - $T_C$ = 25°C | (Note 1a) | 1.6 | W |
| | | - $T_A$ = 25°C | (Note 1b) | 0.4 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | | -55 to +150 | °C |

### Thermal Characteristics

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | (Note 1) | 3.5 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 55 | |

### Package Marking and Ordering Information

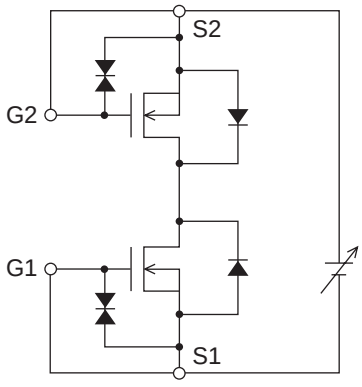
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| MT4638R | MT4638R | CSP | - | - | 5000 |

## Electrical Characteristics at Ta=25°C

| Parameter | Symbol | Conditions | | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|
| Source-to-Source Breakdown Voltage | $V_{(BR)SSS}$ | $I_S$=1mA, $V_{GS}$=0V | Test Circuit 1 | 20 | | | V |
| Zero-Gate Voltage Source Current | $I_{SSS}$ | $V_{SS}$=20V, $V_{GS}$=0V | Test Circuit 1 | | | 1 | μA |
| Gate-to-Source Leakage Current | $I_{GSS}$ | $V_{GS}$=±8V, $V_{SS}$=0V | Test Circuit 2 | | | ±10 | μA |
| Cutoff Voltage | $V_{GS}$(th) | $V_{SS}$=10V, $I_S$=1mA | Test Circuit 3 | 0.6 | 1.0 | 1.5 | V |
| Forward Transfer Admittance | \| yfs \| | $V_{SS}$=10V, $I_S$=3A | Test Circuit 4 | | 5.4 | | S |
| Static Source-to-Source On-State Resistance | $R_{SS}$(on)1 | $I_S$=6A, $V_{GS}$=4.5V | Test Circuit 5 | | | 38 | mΩ |
| | $R_{SS}$(on)2 | $I_S$=5A, $V_{GS}$=2.5V | Test Circuit 5 | | | 48 | mΩ |
| | $R_{SS}$(on)3 | $I_S$=4A, $V_{GS}$=1.8V | Test Circuit 5 | | | 64 | mΩ |
| | | | | | | | |
| Turn-ON Delay Time | $t_d$(on) | See specified Test Circuit. | Test Circuit 7 | | 151 | | ns |
| Rise Time | $t_r$ | See specified Test Circuit. | Test Circuit 7 | | 494 | | ns |
| Turn-OFF Delay Time | $t_d$(off) | See specified Test Circuit. | Test Circuit 7 | | 1447 | | ns |
| Fall Time | $t_f$ | See specified Test Circuit. | Test Circuit 7 | | 812 | | ns |
| Total Gate Charge | Qg | $V_{SS}$=10V, $V_{GS}$=4.5V, $I_S$=6A | | | 7.9 | | nC |
| Forward Source-to-Source Voltage | $V_{F(S-S)}$ | $I_S$=6A, $V_{GS}$=0V | Test Circuit 6 | | | 0.75 | V |

Test circuits are example of measuring FET1 side

Test Circuit 1
$V_{SSS}$ / $I_{SSS}$

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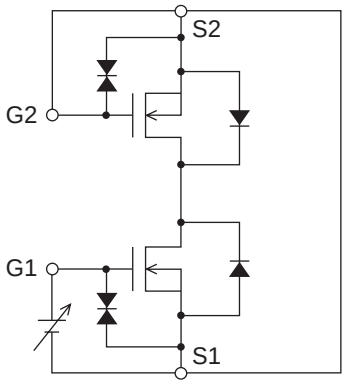
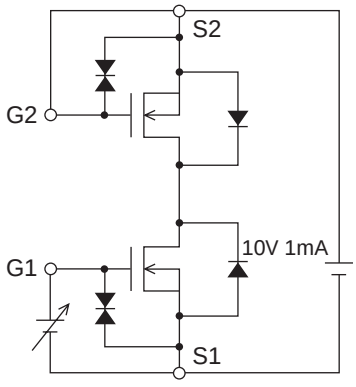
Test Circuit 2
$I_{GSS}$(+) / (--)



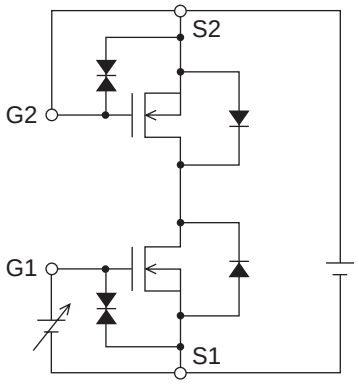

IT11566

Test Circuit 3
$V_{GS}$(th)




IT11567

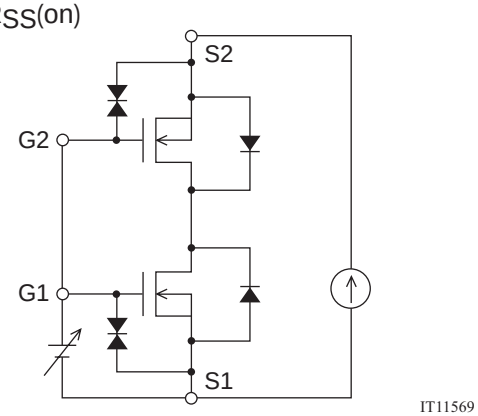
Test Circuit 4
| yfs |



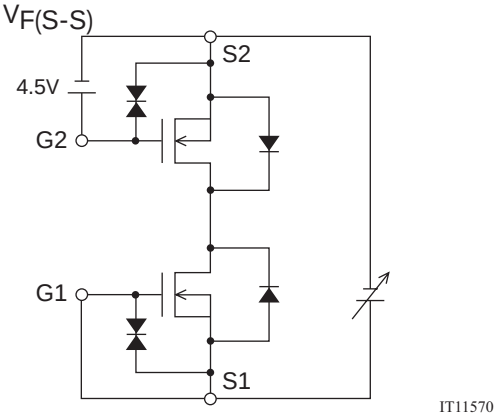

IT11568

* Note: Connect the mesurement terminal reversely if you want to measure the FET2 side.

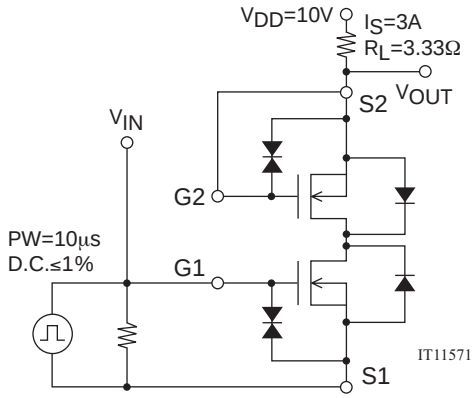
Test Circuit 5
$R_{SS}(on)$



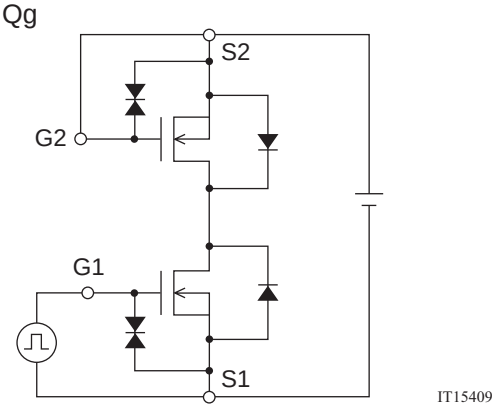

Test Circuit 6
$V_{F(S-S)}$



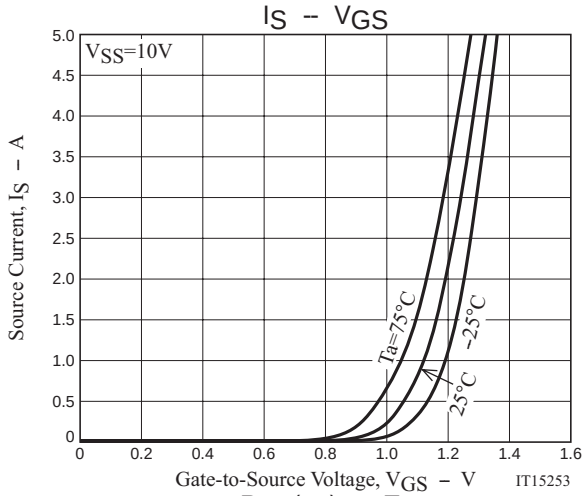

Test Circuit 7
$t_{d(on)}$, $t_r$, $t_{d(off)}$, $t_f$

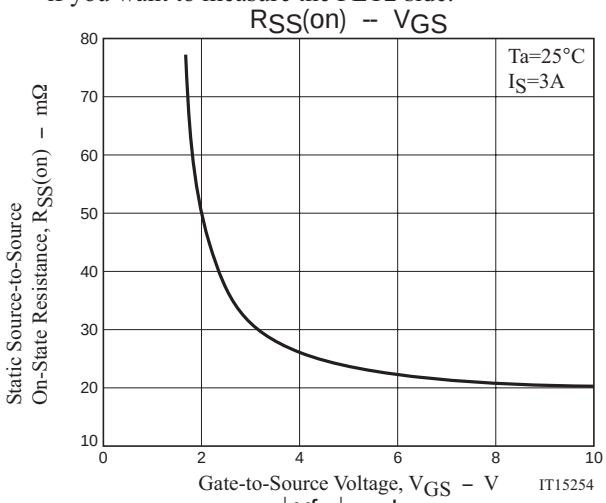


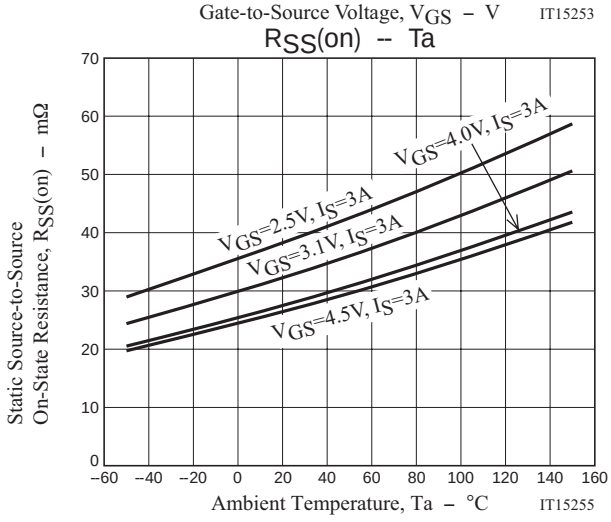

Test Circuit 8
Qg

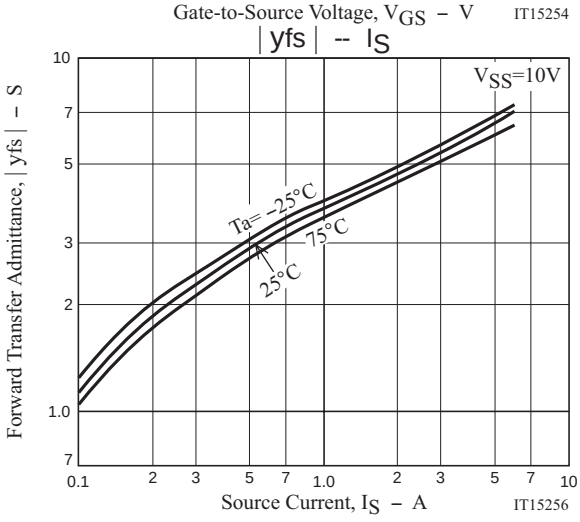


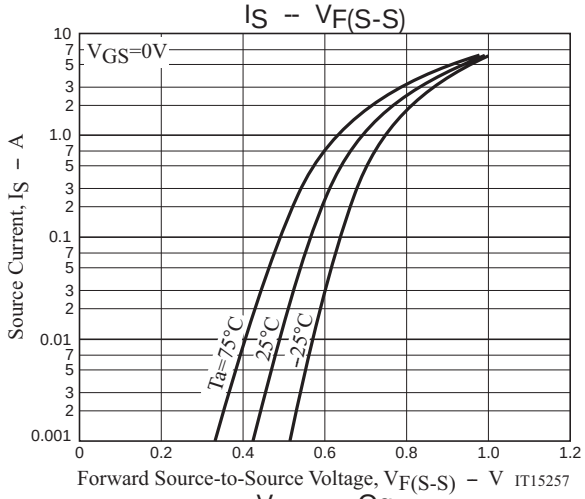

* Note: Connect the mesurement terminal reversely if you want to measure the FET2 side.

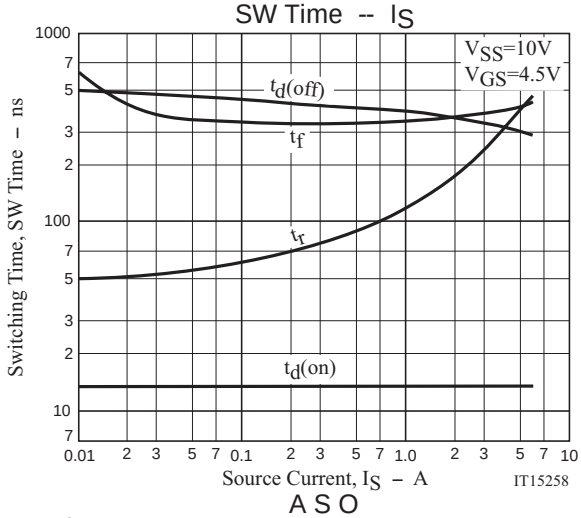


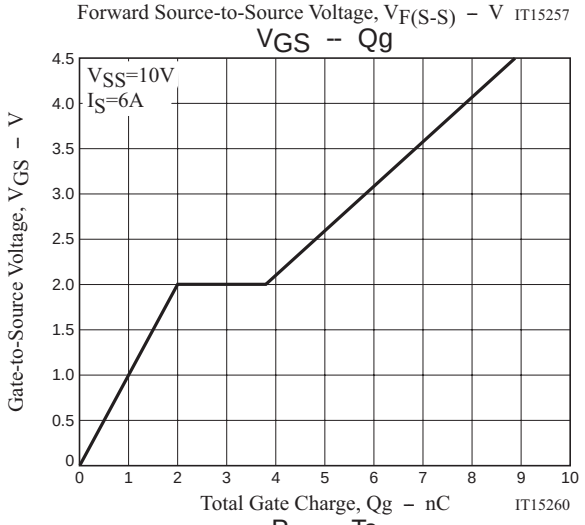



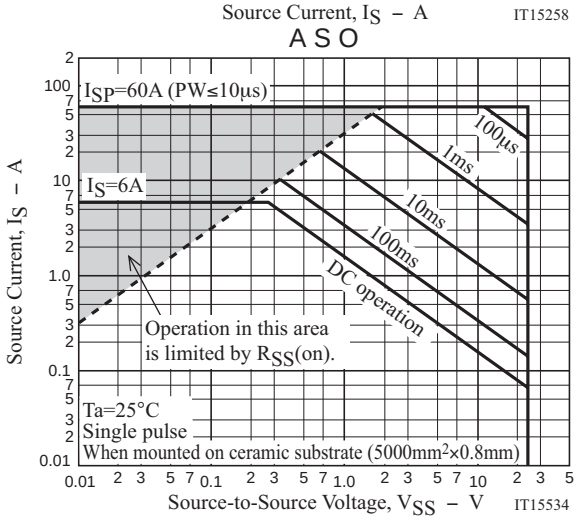



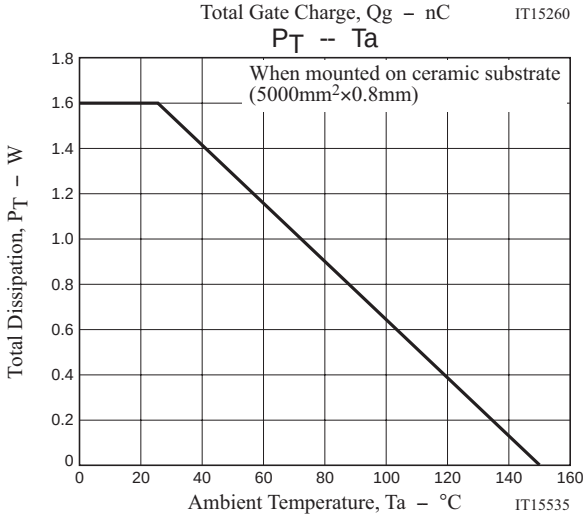




IS – VF(S-S)
VGS=0V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Forward Source-to-Source Voltage, VF(S-S) – V
IT15257


SW Time -- IS
VSS=10V
VGS=4.5V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Source Current, IS – A
IT15258

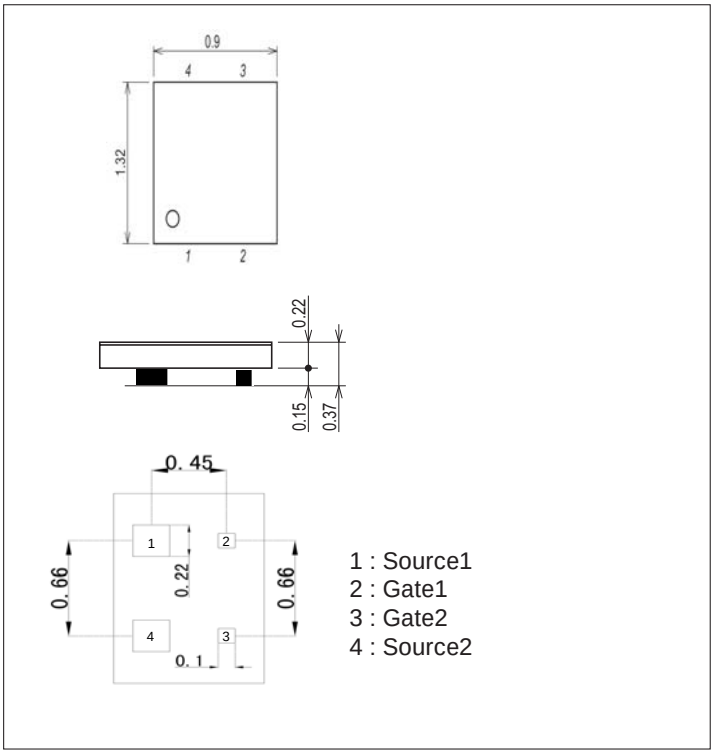

VGS – Qg
VSS=10V
IS=6A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT15260


A S O
ISP=60A (PW≤10μs)
IS=6A
100μs
1ms
10ms
100ms
DC operation
Operation in this area
is limited by RSS(on).
Ta=25°C
Single pulse
When mounted on ceramic substrate (5000mm2×0.8mm)
Source Current, IS – A
Source-to-Source Voltage, VSS – V
IT15534


PT -- Ta
When mounted on ceramic substrate
(5000mm2×0.8mm)
Total Dissipation, PT – W
Ambient Temperature, Ta – °C
IT15535

## Package Dimensions

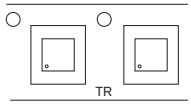
unit : mm (typ)



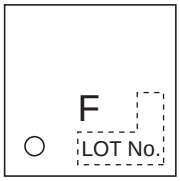

## Product & Package Information

- Package : EFCP
- JEITA, JEDEC : -
- Minimum Packing Quantity : 5,000 pcs./reel

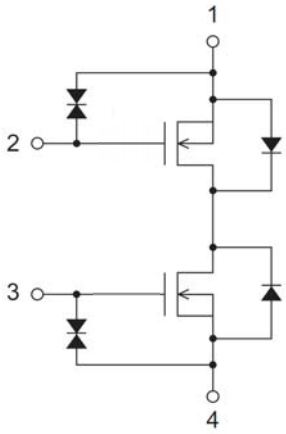
## Taping Type : TR




## Marking




## Electrical Connection



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### Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.