

MT4623

Dual N & P-Channel PowerTrench® MOSFET

General Description

These dual N and P-Channel enhancement mode power field effect transistors are produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

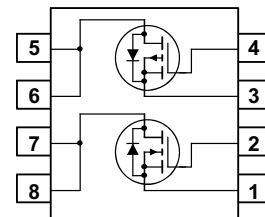
- N-Channel
20V/5A
 $R_{DS(on)} = 0.017\Omega @ V_{GS} = 4.5V$
 $R_{DS(on)} = 0.020\Omega @ V_{GS} = 2.5V$
- P-Channel
-15V/-6A
 $R_{DS(on)} = 0.021\Omega @ V_{GS} = -4.5V$
 $R_{DS(on)} = 0.028\Omega @ V_{GS} = -2.5V$



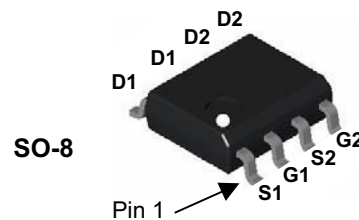
MT Semiconductor®

<http://www.mtsemi.com>

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-CH	P-CH	Units
V _{DSS}	Drain-Source Voltage	20	-15	V
V _{GSS}	Gate-Source Voltage	±10	±12	V
I _D	Drain Current - Continuous			

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MT4623	MT4623	13"	12mm	2500 units

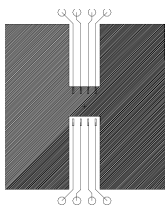
N-CH Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	20	21.5	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±10V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	0.5	0.70	1.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =2.5V, I _D =4.5 A	-	20	35	mΩ
		V _{GS} =4.5V, I _D =5A	-	17	28	mΩ
Forward Transconductance	g _{FS}	V _{DS} =15V,I _D =5A	25	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =10V,V _{GS} =0V, F=1.0MHz	-	780	-	PF
Output Capacitance	C _{oss}		-	140	-	PF
Reverse Transfer Capacitance	C _{rss}		-	80	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V,I _D =1A V _{GS} =4.5V,R _{GEN} =6Ω	-	9	-	nS
Turn-on Rise Time	t _r		-	30	-	nS
Turn-Off Delay Time	t _{d(off)}		-	35	-	nS
Turn-Off Fall Time	t _f		-	10	-	nS
Total Gate Charge	Q _g	V _{DS} =10V,I _D =5A,V _{GS} =4.5V	-	11.4	-	nC
Gate-Source Charge	Q _{gs}		-	2.3	-	nC
Gate-Drain Charge	Q _{gd}		-	2.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =1A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	5	A

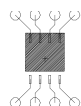
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

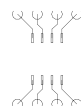
$R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°/W when mounted on a 0.5 in² pad of 2 oz copper



b) 125°/W when mounted on a .02 in² pad of 2 oz copper



c) 135°/W when mounted on a minimum pad.

P-CH Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-15	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-12V,V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 6)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250μA	-0.4	-0.65	-1.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-6A	-	21	30	mΩ
		V _{GS} =-2.5V, I _D =-5A	-	28	45	
Forward Transconductance	g _{FS}	V _{DS} =-5V,I _D =-6A		17	-	S
Dynamic Characteristics (Note7)						
Input Capacitance	C _{iss}	V _{DS} =-6V,V _{GS} =0V, F=1.0MHz	-	1100	-	PF
Output Capacitance	C _{oss}		-	390	-	PF
Reverse Transfer Capacitance	C _{rss}		-	300	-	PF
Switching Characteristics (Note 7)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-6V,I _D =-1A , R _L =6Ω,V _{GEN} =-4.5V,R _g =6Ω	-	25	-	nS
Turn-on Rise Time	t _r		-	45	-	nS
Turn-Off Delay Time	t _{d(off)}		-	72	-	nS
Turn-Off Fall Time	t _f		-	60	-	nS
Total Gate Charge	Q _g	V _{DS} =-6V,I _D =-6A,V _{GS} =-4.5V	-	11.5	-	nC
Gate-Source Charge	Q _{gs}		-	1.5	-	nC
Gate-Drain Charge	Q _{gd}		-	3.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 6)	V _{SD}	V _{GS} =0V,I _S =-1.0A	-	-	-1.2	V
Diode Forward Current (Note 5)	I _S		-	-	-6	A

Notes:

5. Surface Mounted on FR4 Board, $t \leq 10$ sec.
6. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
7. Guaranteed by design, not subject to production

N- Channel Typical Electrical and Thermal Characteristics (Curves)

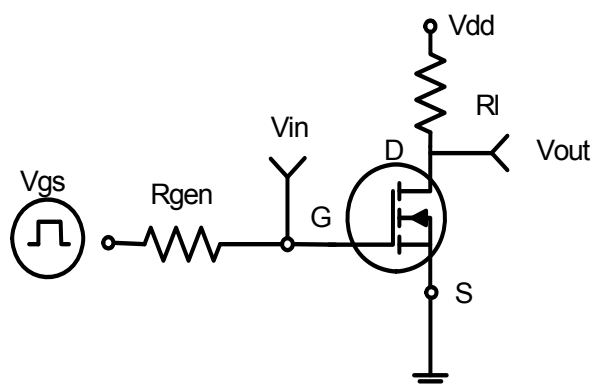


Figure 1: Switching Test Circuit

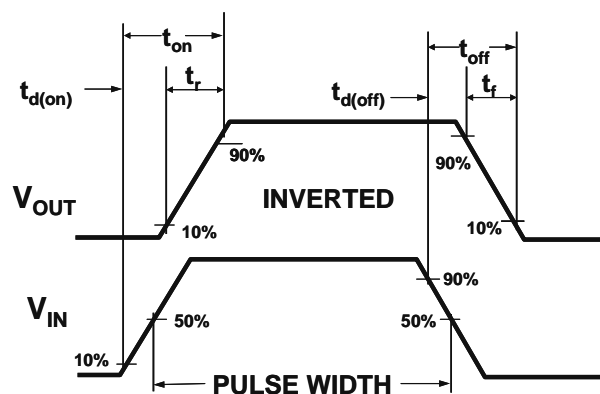


Figure 2: Switching Waveforms

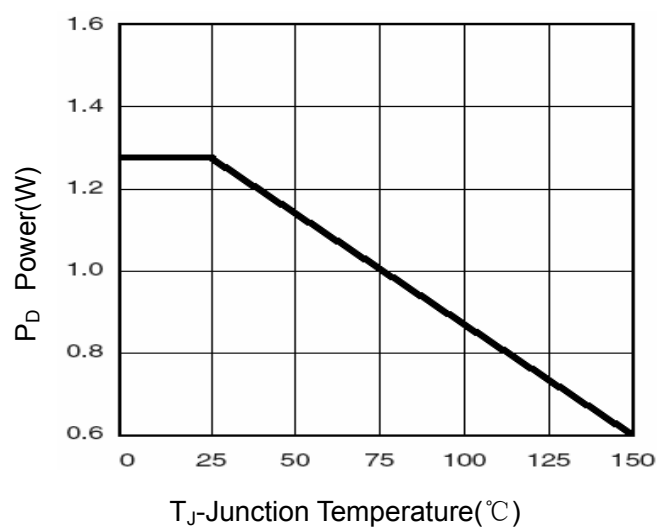


Figure 3 Power Dissipation

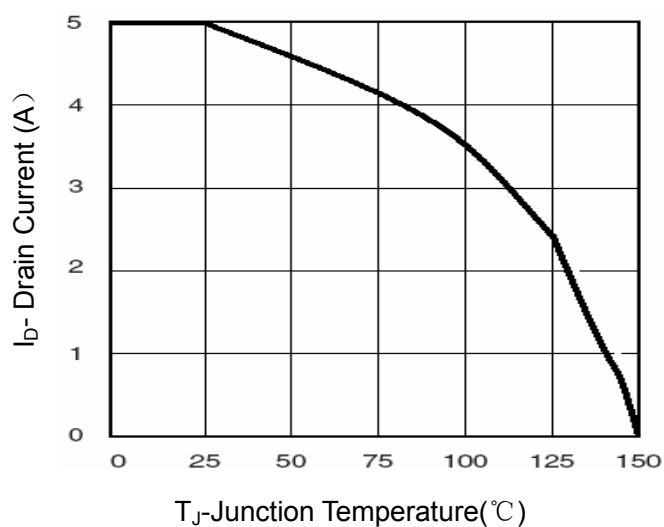


Figure 4 Drain Current

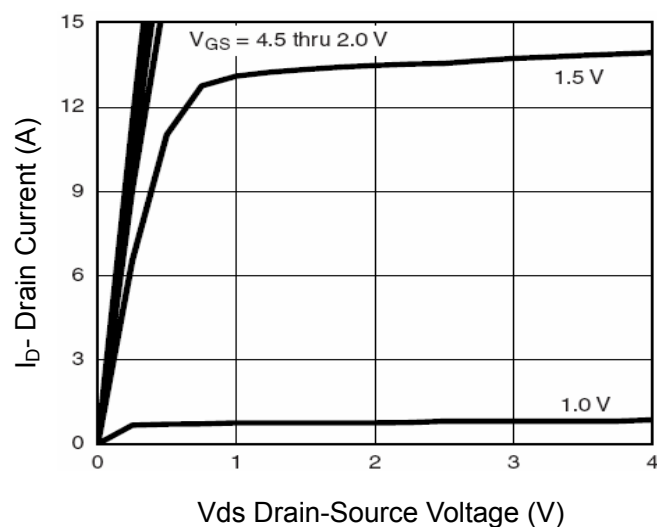


Figure 5 Output Characteristics

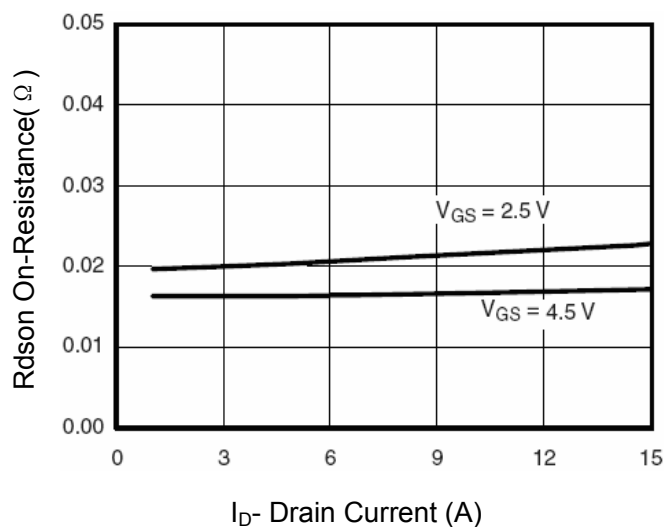


Figure 6 Drain-Source On-Resistance

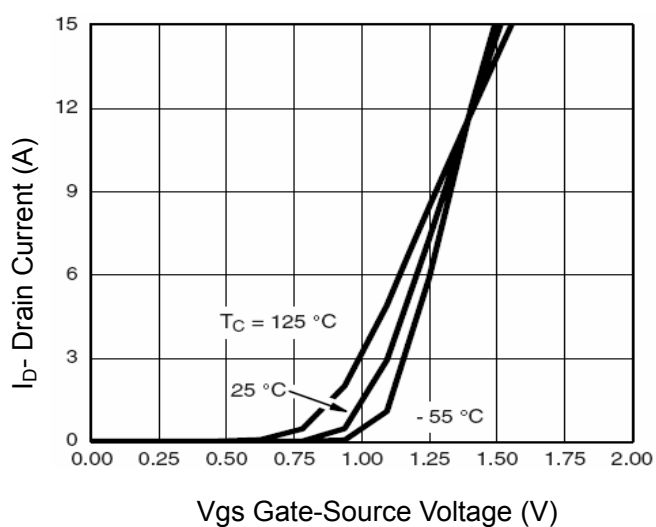


Figure 7 Transfer Characteristics

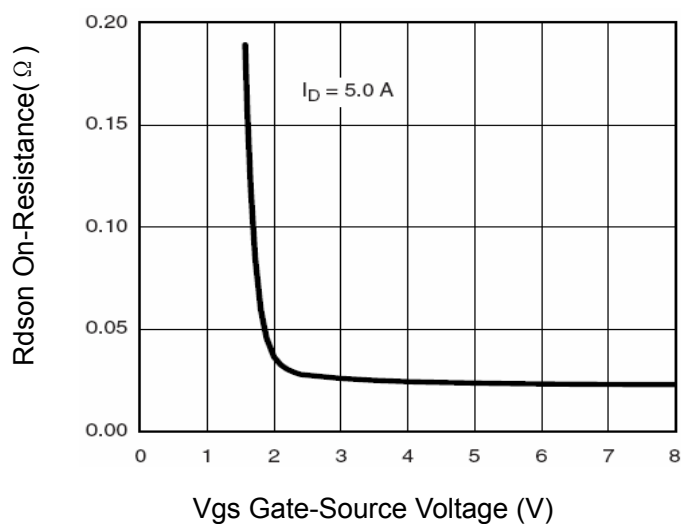


Figure 9 Rdson vs Vgs

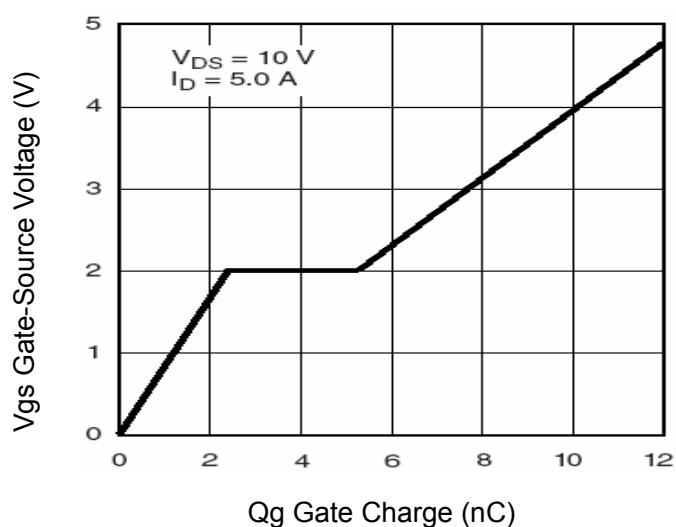


Figure 11 Gate Charge

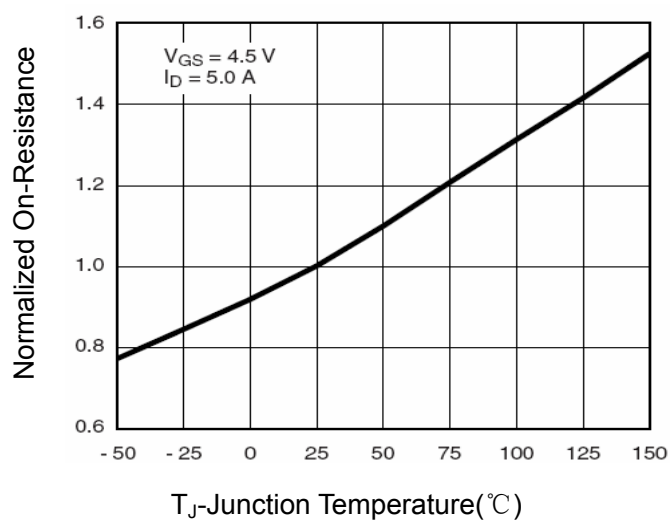


Figure 8 Drain-Source On-Resistance

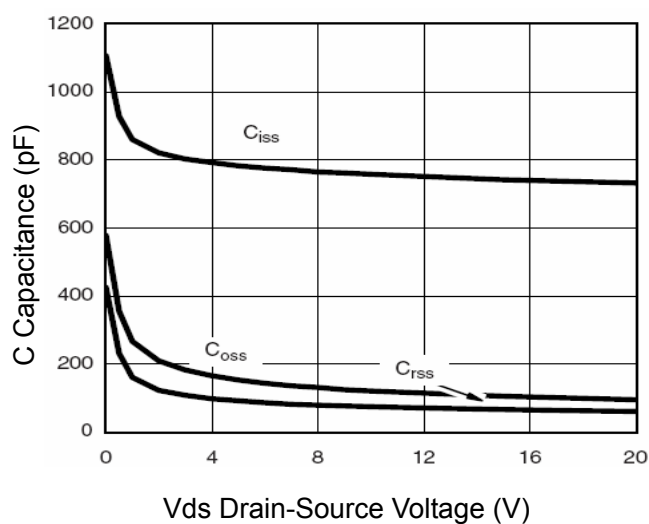


Figure 10 Capacitance vs Vds

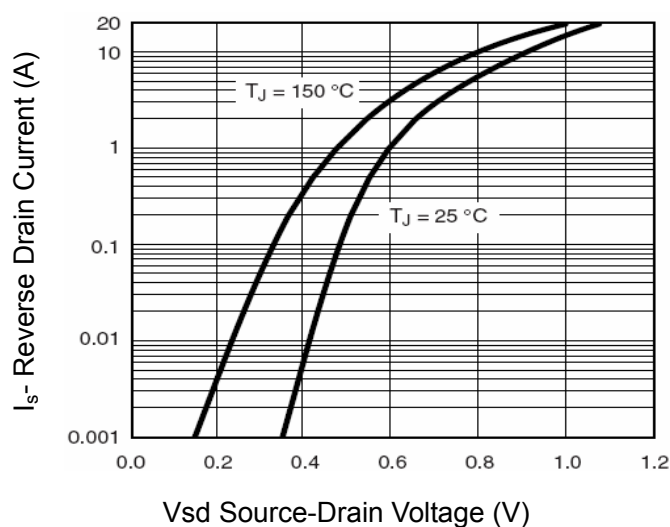


Figure 12 Source- Drain Diode Forward

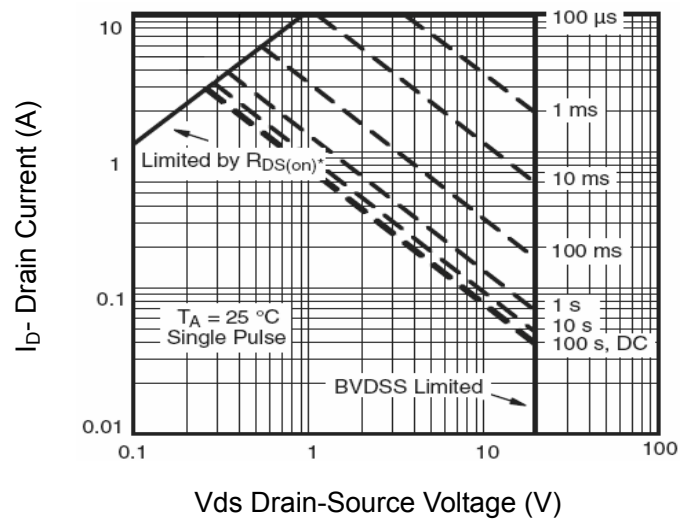


Figure 13 Safe Operation Area

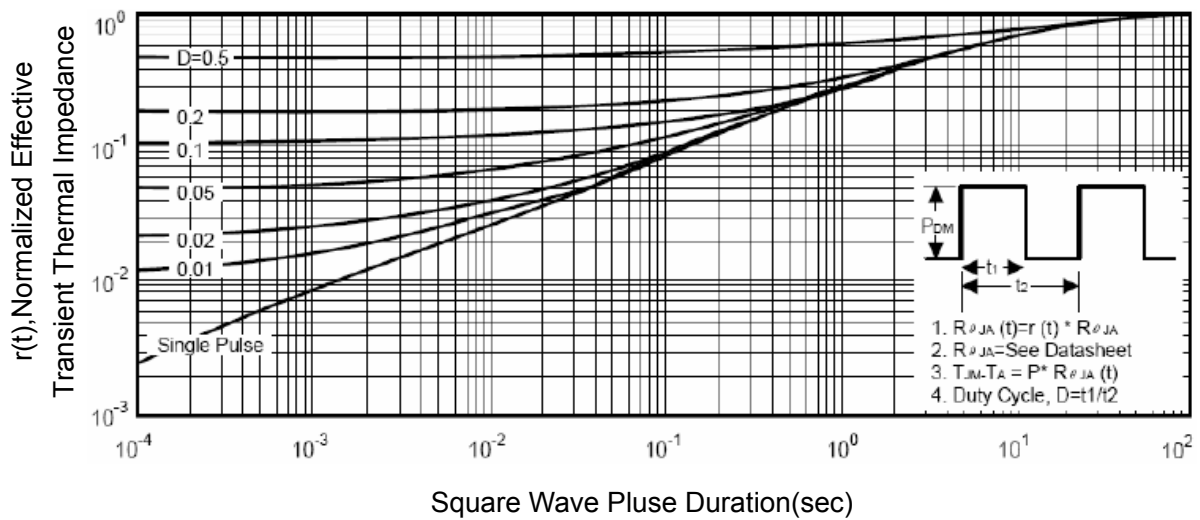


Figure 14 Normalized Maximum Transient Thermal Impedance

P- Channel Typical Electrical and Thermal Characteristics (Curves)

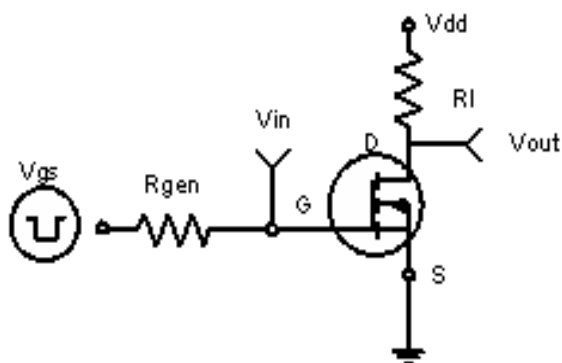


Figure 1: Switching Test Circuit

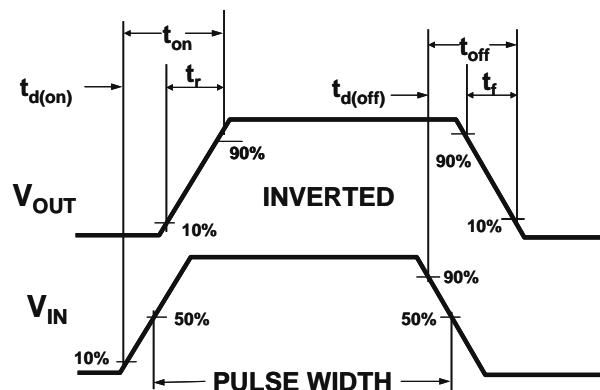


Figure 2: Switching Waveforms

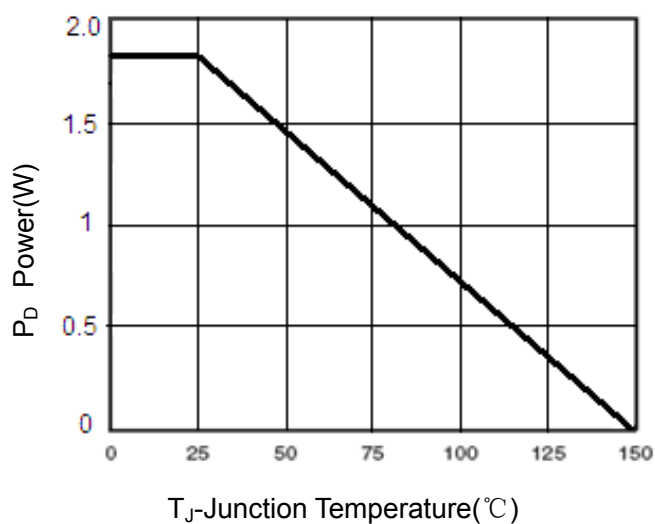


Figure 3 Power Dissipation

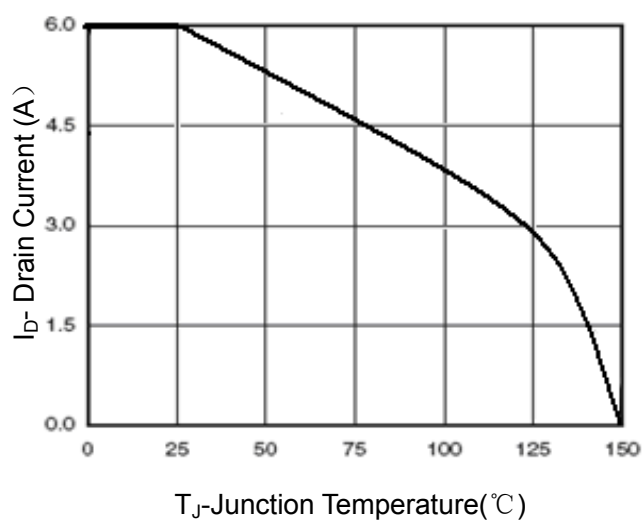


Figure 4 Drain Current

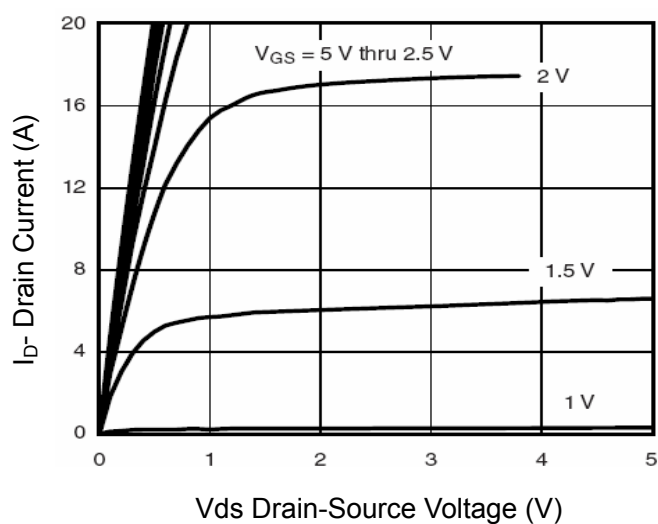


Figure 5 Output Characteristics

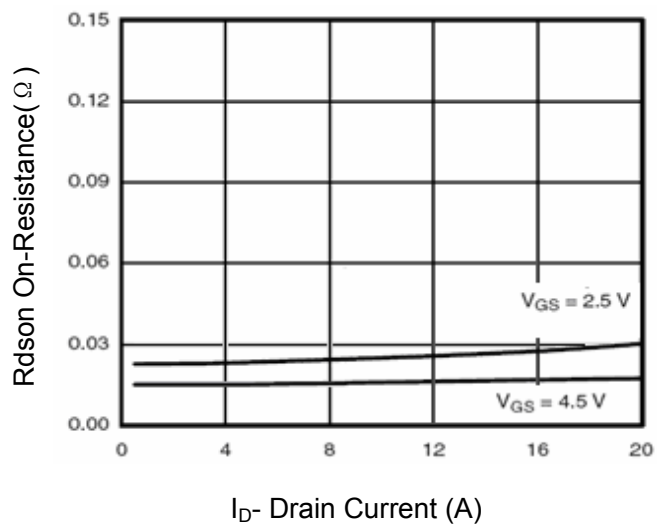


Figure 6 Drain-Source On-Resistance

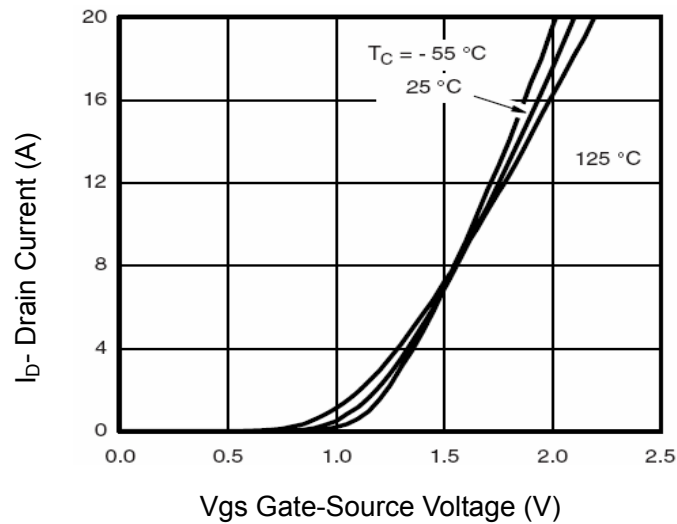


Figure 7 Transfer Characteristics

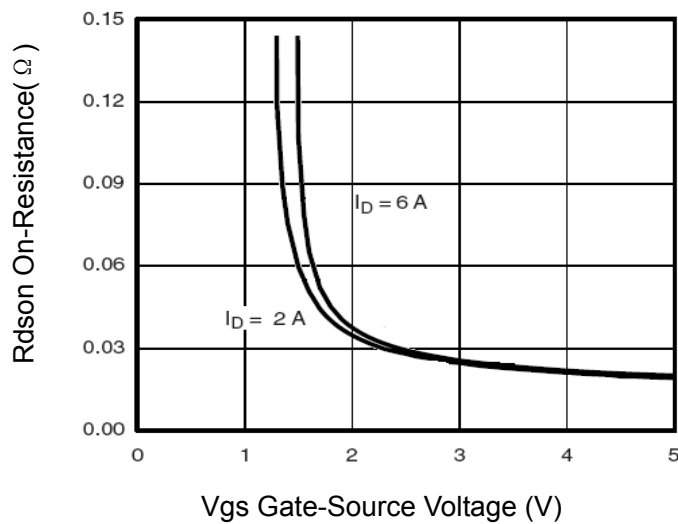


Figure 9 Rdson vs Vgs

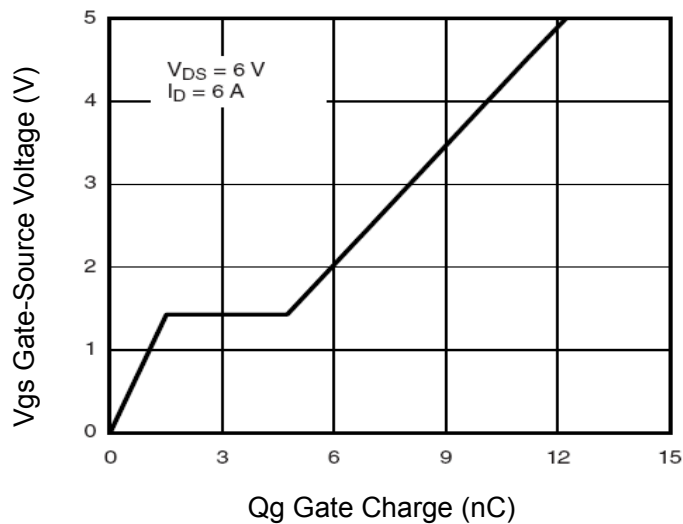


Figure 11 Gate Charge

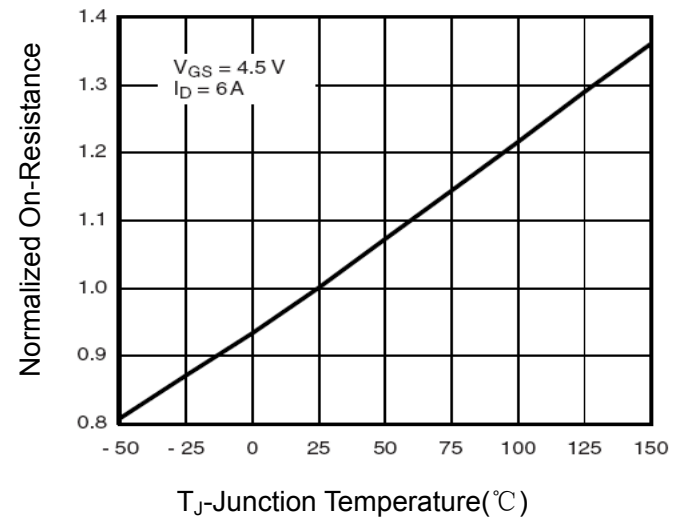


Figure 8 Drain-Source On-Resistance

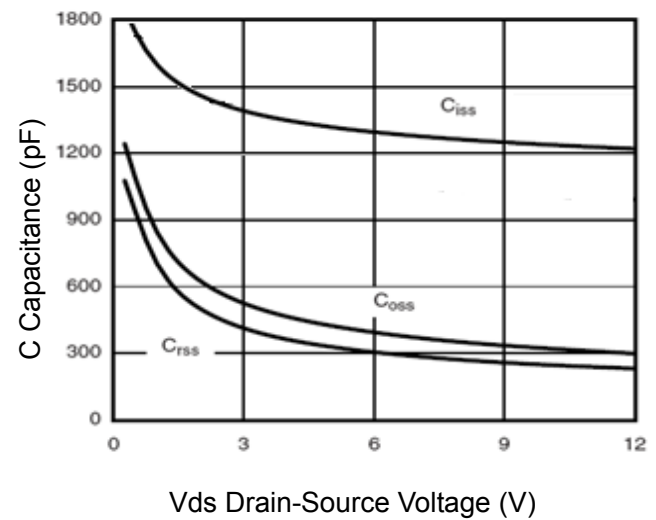


Figure 10 Capacitance vs Vds

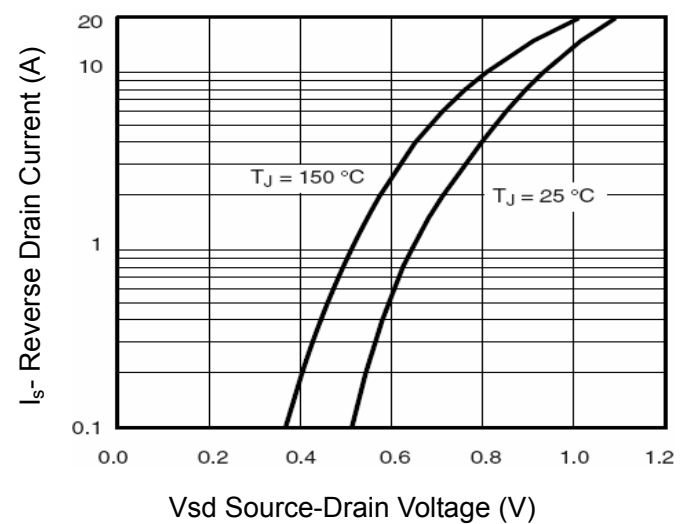


Figure 12 Source- Drain Diode Forward

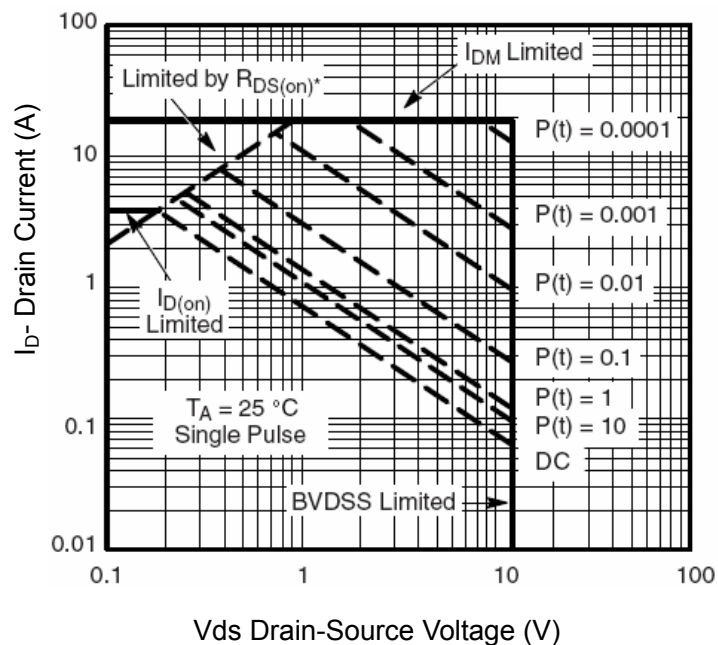


Figure 13 Safe Operation Area

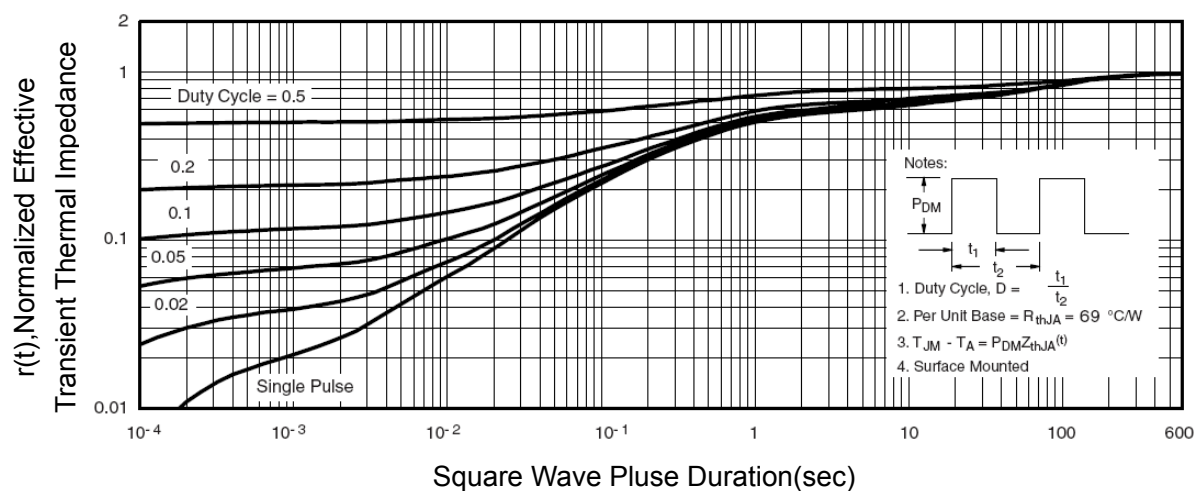


Figure 14 Normalized Maximum Transient Thermal Impedance

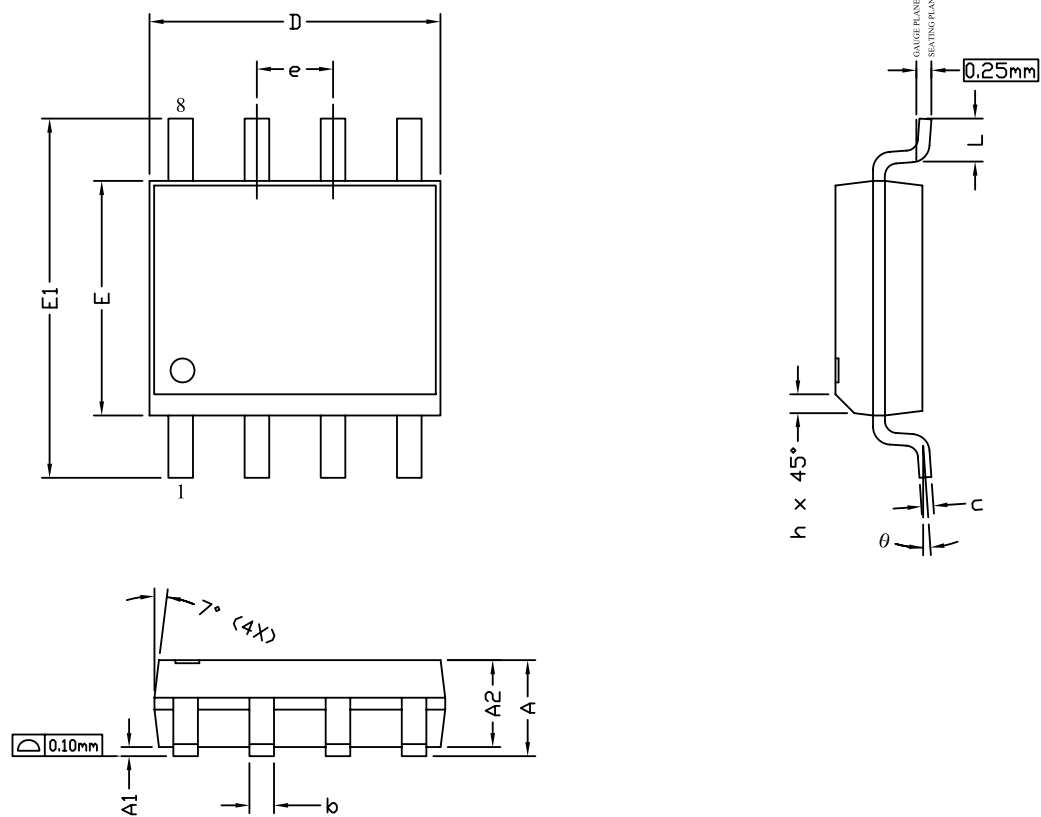
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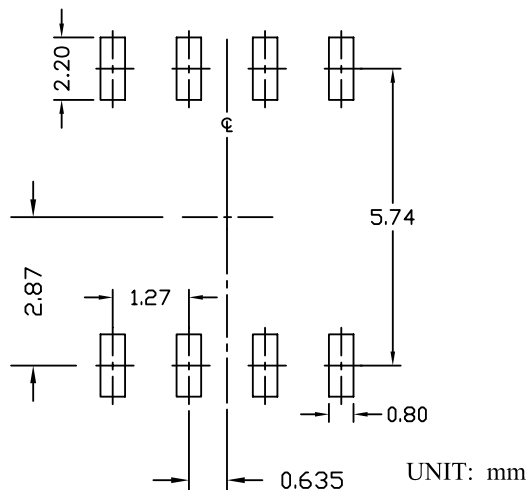
Version

rev H

SO8 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
θ	0°	—	8°	0°	—	8°

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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8. 除上述第7项内容外, 不能将本资料中记载的产品用于以下用途。如果用于以下用途而造成的损失, 本公司概不负责。
 - 1) 生命维持装置。
 - 2) 植埋于人体使用的装置。
 - 3) 用于治疗(切除患部、给药等)的装置。
 - 4) 其他直接影响到人的生命的装置。
9. 在使用本资料所记载的产品时, 对于最大额定值、工作电源电压的范围、放热特性、安装条件及其他条件请在本公司规定的保证范围内使用。如果超出了本公司规定的保证范围使用时, 对于由此而造成的故障和出现的事, 本公司将不承担任何责任。
10. 本公司一直致力于提高产品的质量和可靠性, 但一般来说, 半导体产品总会以一定的概率发生故障、或者由于使用条件不同而出现错误运行等。为了避免因本公司的产品发生故障或者错误运行而导致人身事故和火灾或造成社会性的损失, 希望客户能自行负责进行冗余设计、采取延烧对策及进行防止错误运行等的安全设计(包括硬件和软件两方面的设计)以及老化处理等, 这是作为机器和系统的出厂保证。特别是单片机的软件, 由于单独进行验证很困难, 所以要求在顾客制造的最终的机器及系统上进行安全检验工作。
11. 如果把本资料所记载的产品从其载体设备上卸下, 有可能造成婴儿误吞的危险。顾客在将本公司产品安装到顾客的设备上时, 请顾客自行负责将本公司产品设置为不容易剥落的安全设计。如果从顾客的设备上剥落而造成事故时, 本公司将不承担任何责任。
12. 在未得到本公司的事先书面认可时, 不可将本资料的一部分或者全部转载或者复制。
13. 如果需要了解关于本资料的详细内容, 或者有其他关心的问题, 请向本公司的营业窗口咨询。

Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.